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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/531,105	03/17/2000	Shinkichi Gama	1614.1040	5186

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EXAMINER	
ARANI, TAGHI T	
ART UNIT	**PAPER NUMBER**
2131	

DATE MAILED: 09/07/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/531,105	GAMA ET AL.	
	Examiner	Art Unit	
	Taghi T. Arani	2131	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on *25 May 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-10 are pending for examination.

Response to Amendment

2. Applicant's amendment filed 5/25/2005 necessitated the new ground(s) of rejection presented in this Office action. Accordingly, THIS ACTION IS MADE FINAL. See MPEP 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1-10 are rejected under 35 U.S.C. 102 (e) as being unpatentable over Nakamura et al., US Patent No. 6,457,126 (prior art of record).

As per claim 1, Nakamura et al. teach a storage device for maintaining information which is accessed by a host device through a host interface when power is OFF and being capable of executing a test process based on test signals (Figure 1, col. 7, lines 21-65), comprising:

a memory including a plurality of memory locations and storing secret data (Figure1 and associated text, storage device 10 including Flash memory 11, first ROM13, second ROM 14 and SRAM15, Figure 2, wherein secret data is stored in memory location T1, a system key in

memory location T2 and an expected value at the memory location T4 (Figure 2 and associated text) or initial data (col. 11, lines 36-45, i.e. the test for the flash memory is performed by checking whether data "0" is stored in its entirty):

a test terminal inputting the test signals indicating a memory location among the plurality of memory locations (Figure 1, test device 30, col., 11, lines 28-45, see also Figure 5 and associated text);

an instruction part sending a read out instruction for instructing the memory storing secret data to read out data stored at the memory location (col. 11, lines 36-65, the controlling section 162 tests the SRAM 13 and ROM 14 by reading the stored data, see also Figure 1 and associated text);

a decoding part decoding whether the data read out by the memory stored at the memory location in response to the data reading instruction is the secret data or the initial data (col. 12, lines 5-12, see also col. 13, lines 13-19);

a maintaining part maintaining information in a volatile state resulting from the decoding part (col. 12, lines 5-12, i.e. the address counter 163) ; and

a cutting-off part cutting off the test signals input from the test terminal when the maintaining part maintains information indicating that the secret data is stored at the memory location (col. 12, lines 55-62, see also col. 13, lines 20-25, i.e. when the system key area T2 and the decrypting program T3 (i.e. secrete data) are addressed , it is preferred that the second ROM 15 be set in a disable state (i.e. cutting off the test signal)).

As per claim 2, Nakamura et al. teach the storage device as claimed in claim 1, wherein said read out instruction sent by said instruction part is a secret data read out instruction for instructing the memory storing secret data to read out the secret data (col. 12, lines 5-12).

As per claim 3, Nakamura et al. teach the storage device as claimed in claim 1, wherein said read out instruction sent by said instruction part is a data read out instruction for instructing the memory storing secret data to read out all data stored in the memory other than working data (col. 12, lines 13-27).

As per claim 4, Nakamura et al. teach the storage device as claimed in claim 1, wherein said read out instruction sent by said instruction part is a data read out instruction for instructing the memory storing secret data to read out data indicating a presence of the secret data stored in an area that is not for the secret data (col. 11, lines 54-65, see also col. 12, lines 28-54).

As per claims 5 and 6 , Nakamura et al. teach the storage device as claimed in claim 1, wherein said instruction part sends the read out instruction when the power is ON; and

wherein said instruction part sends the read out instruction when the memory is reset (col. 20, lines 18-30).

As per claim 7, Nakamura et al. teach the storage device as claimed in claim 1, wherein said instruction part sends the read out instruction when a command for operating secret data is made (col. 11, lines 21-35).

As per claim 8, Nakamura et al. teach a storage device for maintaining information. which is accessed by a host device through a host interface, when the power is OFF and being capable of executing a test process based on test signals (Figure 1, col. 7, lines 21-65), comprising:

a memory including a plurality of memory locations and storing secret data (Figure1, storage device 10 including memory locations Flash memory 11, first ROM13, second ROM 14 and SRAM15, Figure 2, T1 and T2 storing secret data);

a decoding part gathering a set of data read out by the memory storing secret data at a memory location among the plurality of memory locations in response to an access request indicating the memory location and decoding based on the set of data whether or not the secret data is stored at the memory location (col. 11, lines 36-65, Figure 1, the controller 12 and the controlling section 162, col. 12, lines 5-12, col. 13, lines 13-19):

a maintaining part maintaining information in a volatile state resulting from the decoding part (col. 12, lines 5-12, i.e. the address counter 163); and

a cutting-off part cutting off the test signals input from a test terminal when the maintaining pad maintains information indicating that the secret data is stored at the memoœ location (col. 12, lines 55-62, see also col. 13, lines 20-25, i.e. when the system key area T2 and the decrypting program T3 (i.e. secrete data) are addressed , it is preferred that the second ROM 15 be set in a disable state (i.e. cutting off the test signal),).

As per claim 9, Nakamura et al. teach a storage device for maintaining information. which is accessed by a host device through a host interface. when power is OFF and being capable of executing a test process based on test signals (Figure 1, col. 7, lines 21-65), comprising:

a memory including a plurality of memory locations and storing secret data (Figure1, storage device 10 including memory locations Flash memory 11, first ROM13, second ROM 14 and SRAM15, Figure 2, T1 and T2 storing secret data);

a maintaining part maintaining, in a volatile state, information indicating that an access request is conducted to a memory location among the plurality of memory locations storing secret data (col. 12, lines 5-12, i.e. the address counter 163) ; and

a cutting-off part cutting of the test signals input from a test terminal when the maintaining part maintains the information indicating that the access request is conducted to the memory location storing secret data (col. 12, lines 55-62, see also col. 13, lines 20-25, i.e. when the system key area T2 and the decrypting program T3 (i.e. secrete data) are addressed , it is preferred that the second ROM 15 be set in a disable state (i.e. cutting off the test signal)).

As per claim 10, Nakamura et al. teach A storage device for non-volatile storage of information and which executes a test process, the storage device communicating with a host via a host interface, the storage device comprising (Figure 1, col. 7, lines 21-65):

a memory including a plurality of memory locations and storing secret data (Figure1, storage device 10 including memory locations Flash memory 11, first ROM13, second ROM 14 and SRAM15, Figure 2, T1 and T2 storing secret data);

a test terminal which receives at least one test signal indicating a memory location among the plurality of memory locations from which to read out data (Figure 1, TEST DEVICE 30, col. 13, line 65 through col. 14, line 5);

a maintaining part which maintains information about the data stored at the memory location in a volatile state(col. 12, lines 5-12, i.e. the address counter 163);

a cutting-off part which cuts off the at least one test signal from the test terminal when the maintaining part maintains information indicating that the data stored at the memory location

includes secret data (col. 12, lines 55-62, see also col. 13, lines 20-25, i.e. when the system key area T2 and the decrypting program T3 (i.e. secrete data) are addressed , it is preferred that the second ROM 15 be set in a disable state (i.e. cutting off the test signal)).

Action is Final

4. **THIS ACTION IS FINAL**. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Conclusion

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Taghi T. Arani whose telephone number is (571) 272-3787. The examiner can normally be reached on 8:00-5:30 Mon-Fri.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ayaz Sheikh can be reached on (571) 272-3795. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

T.A.

Taghi T. Arani, Ph.D.
Examiner
Art Unit 2131

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